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- (57) ABSTRACT

Related U.S. Application Data

- (62) Division of application No. 11/198,298, filed on Aug. 8, 2005.

- (51) **Int. Cl.**
H01L 21/337 (2006.01)

- (52) U.S. Cl. 438/193; 438/195; 257/E21.421

- (58) **Field of Classification Search** 438/142,
438/192, 193, 268, 137-138, 173, 206, 209,
438/212; 257/170, 409, E21.421

See application file for complete search history.

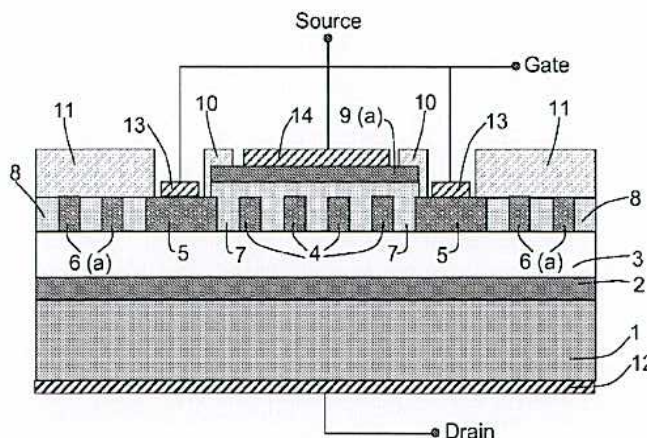
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Semiconductor devices and methods of making the devices are described. The devices can be implemented in SiC and can include epitaxially grown n-type drift and p-type trench gate regions, and an n-type epitaxially regrown channel region on top of the trenched p-gate regions. A source region can be epitaxially regrown on top of the channel region or selectively implanted into the channel region. Ohmic contacts to the source, gate and drain regions can then be formed. The devices can include edge termination structures such as guard rings, junction termination extensions (JTE), or other suitable p-n blocking structures. The devices can be fabricated with different threshold voltages, and can be implemented for both depletion and enhanced modes of operation for the same channel doping. The devices can be used as discrete power transistors and in digital, analog, and monolithic microwave integrated circuits.

14 Claims, 12 Drawing Sheets



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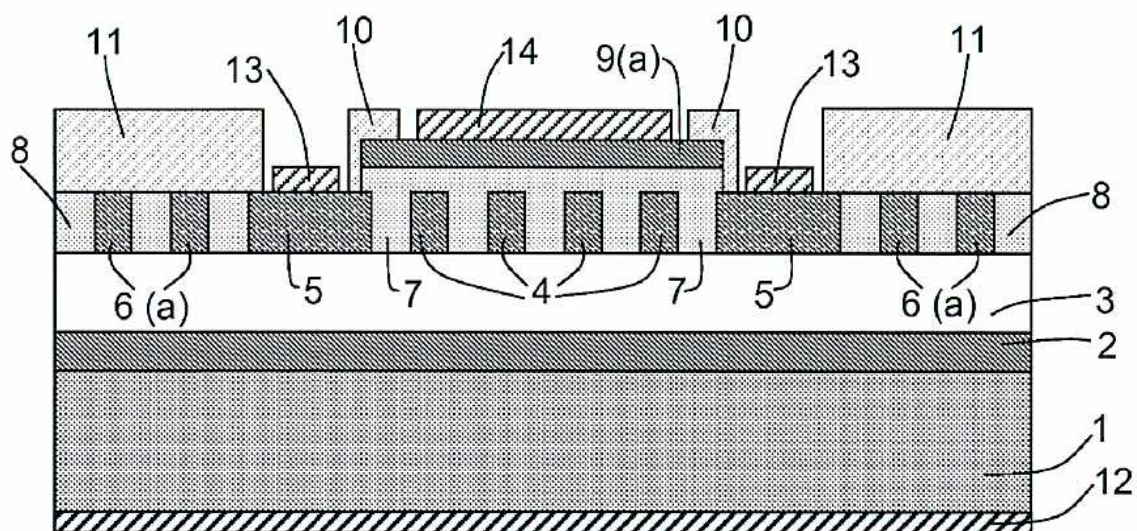
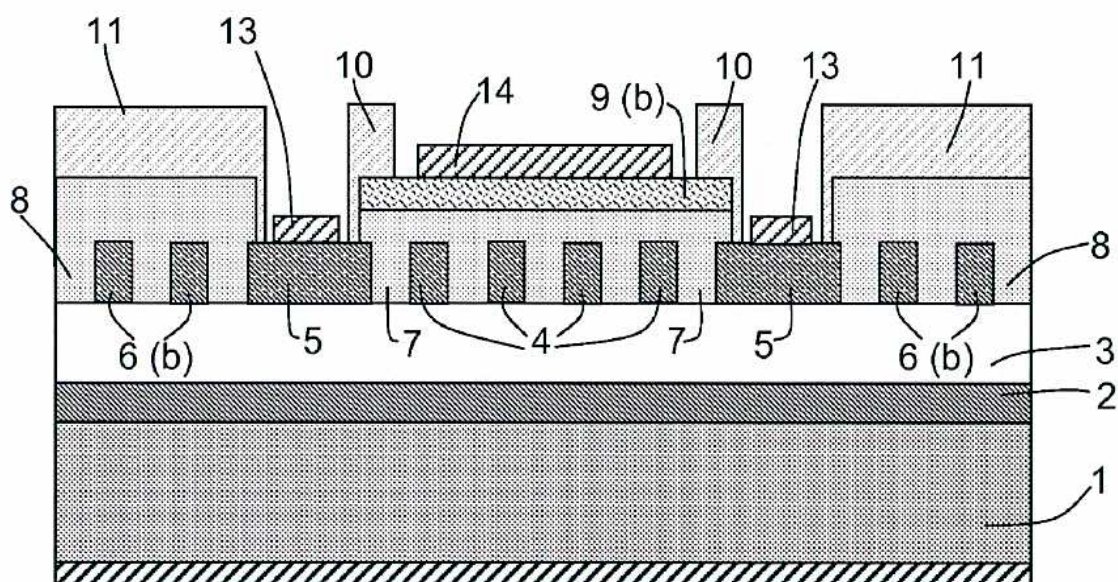
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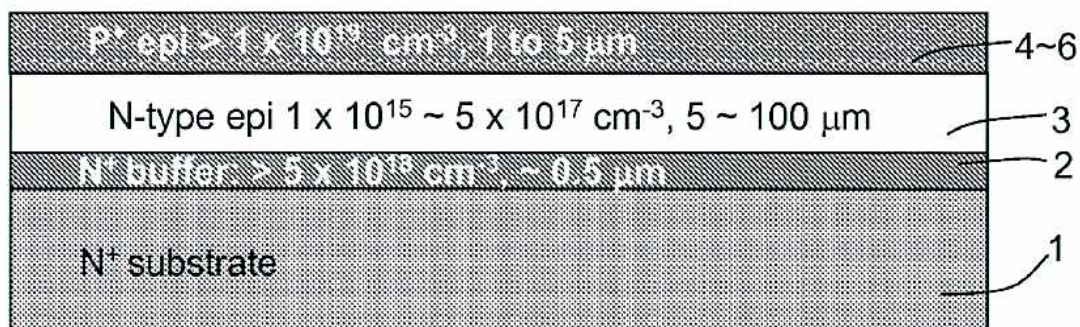
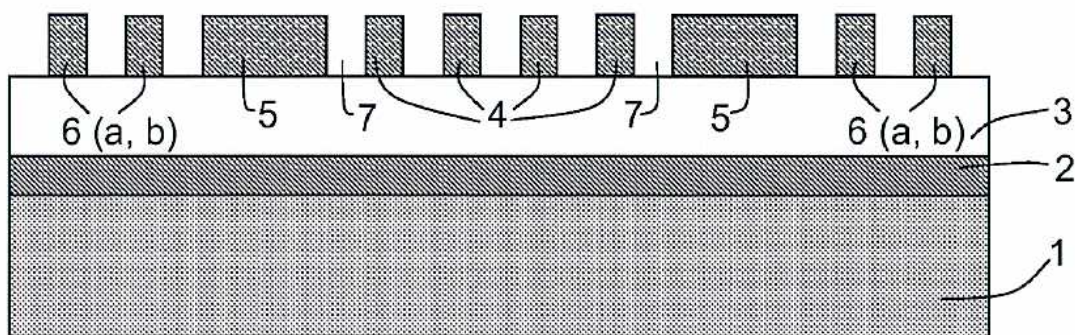
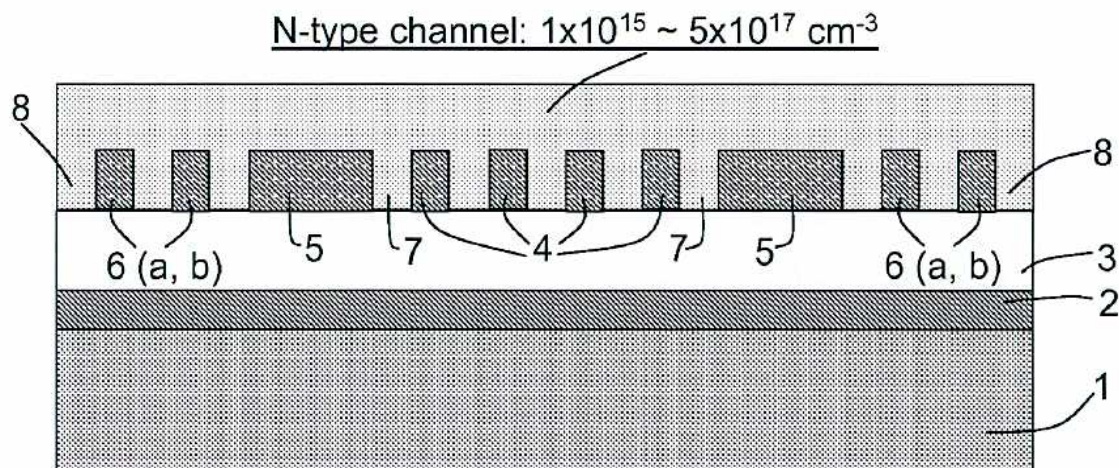
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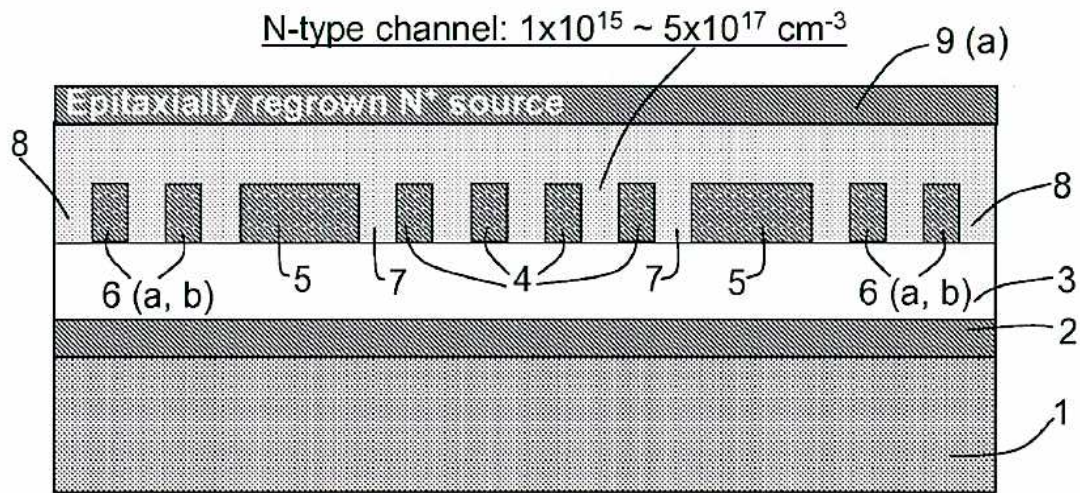
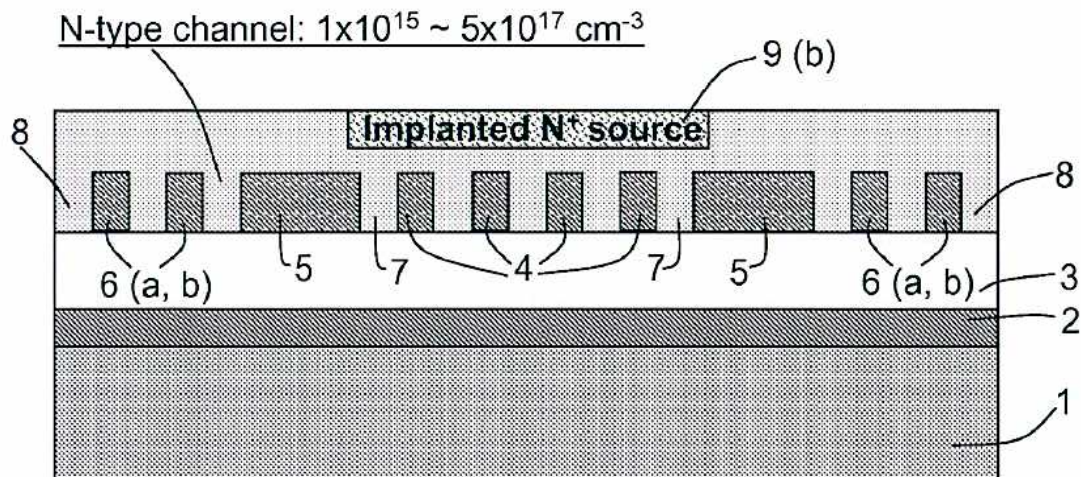
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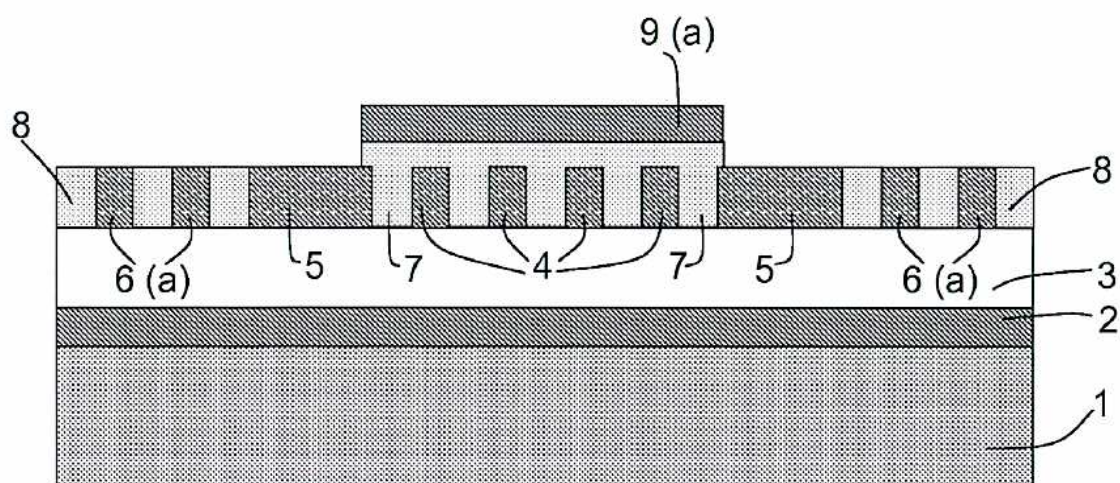
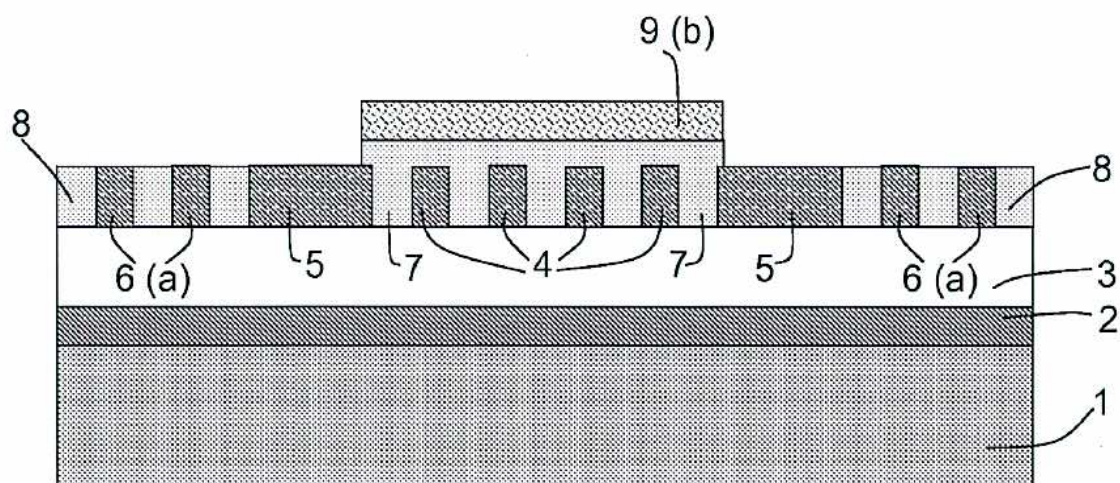
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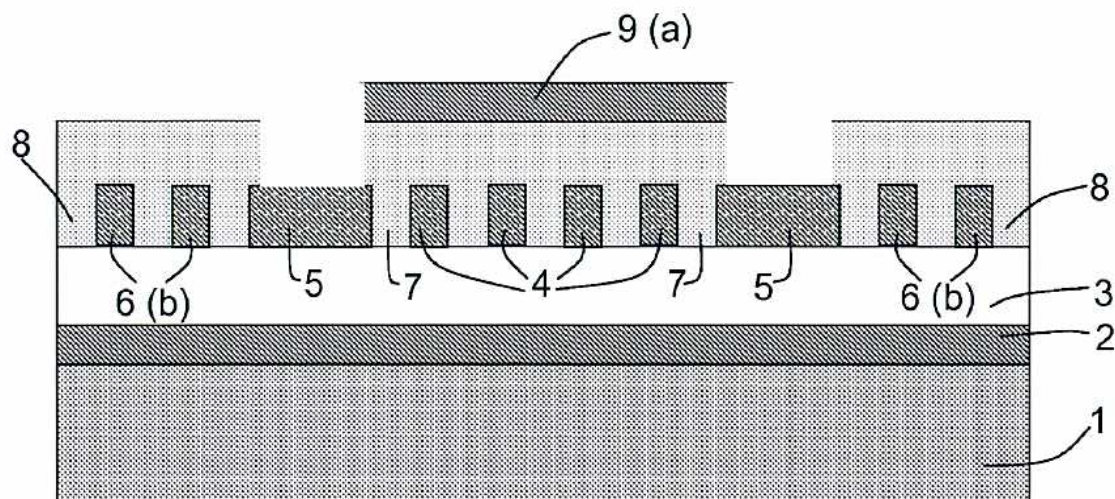
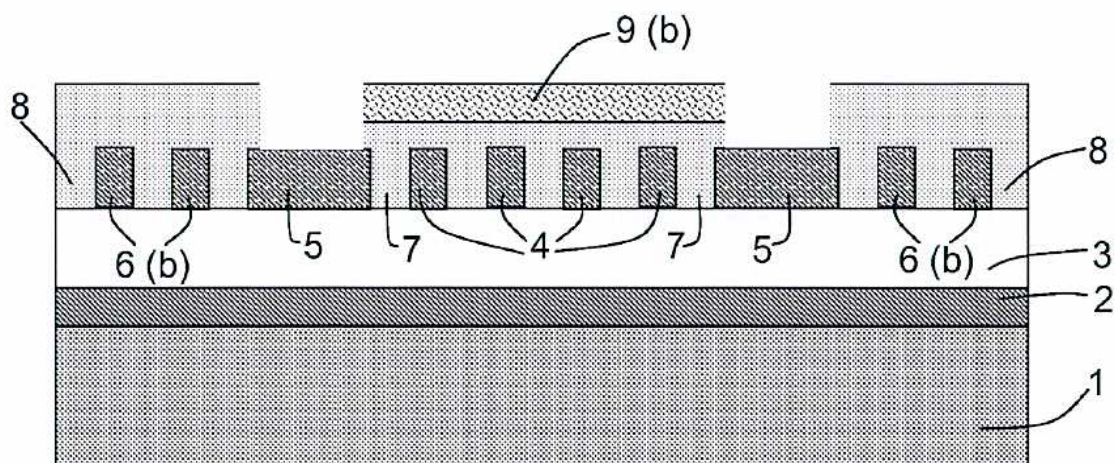
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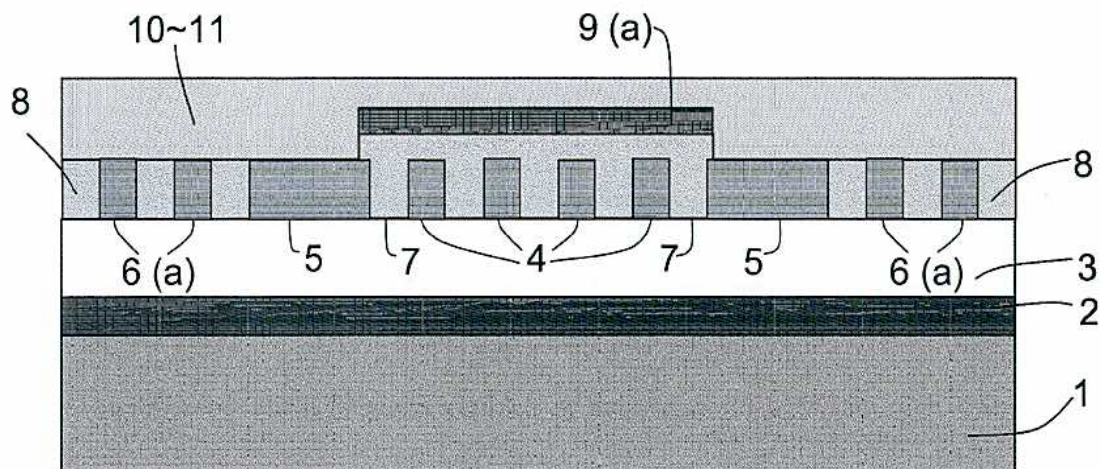
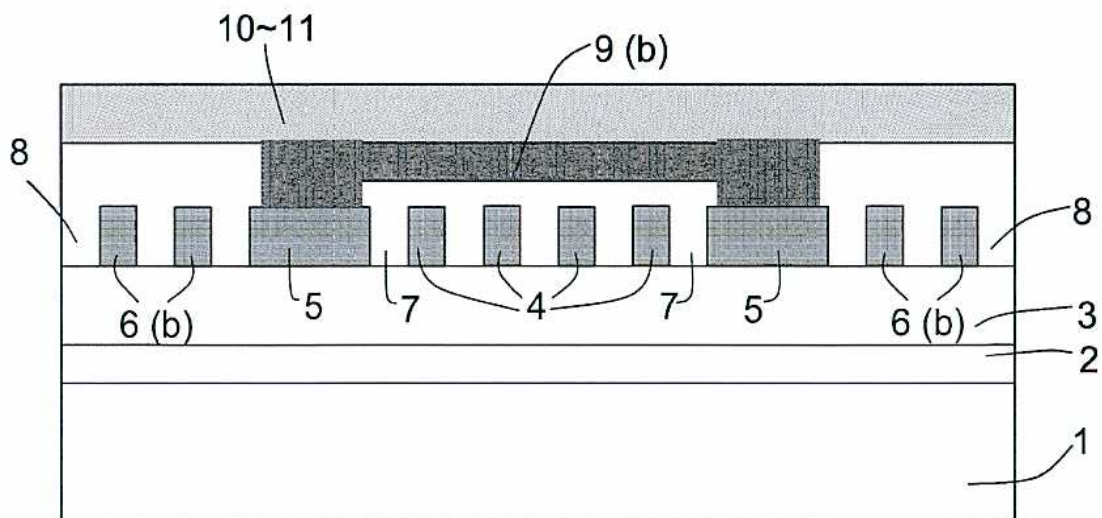
**FIG. 1A****FIG. 1B**

**FIG. 2****FIG. 3****FIG. 4**

**FIG. 5A****FIG. 5B**

**FIG. 6A****FIG. 6B**

**FIG. 6C****FIG. 6D**

**FIG. 7A****FIG. 7B**

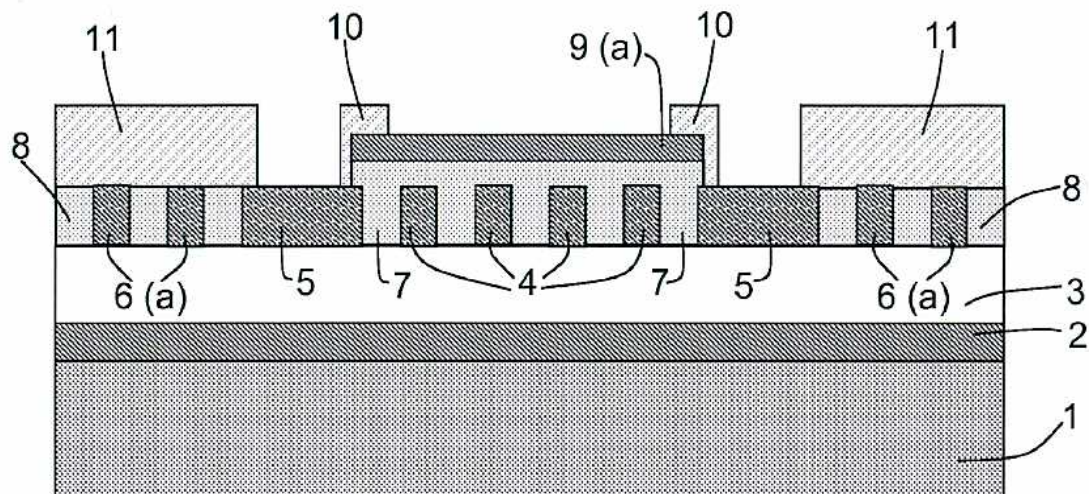


FIG. 8A

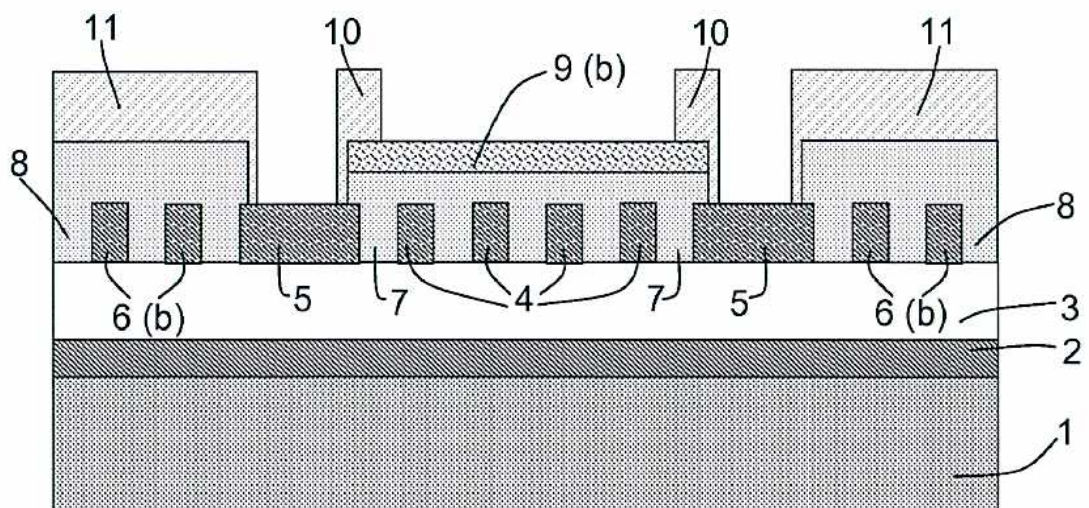
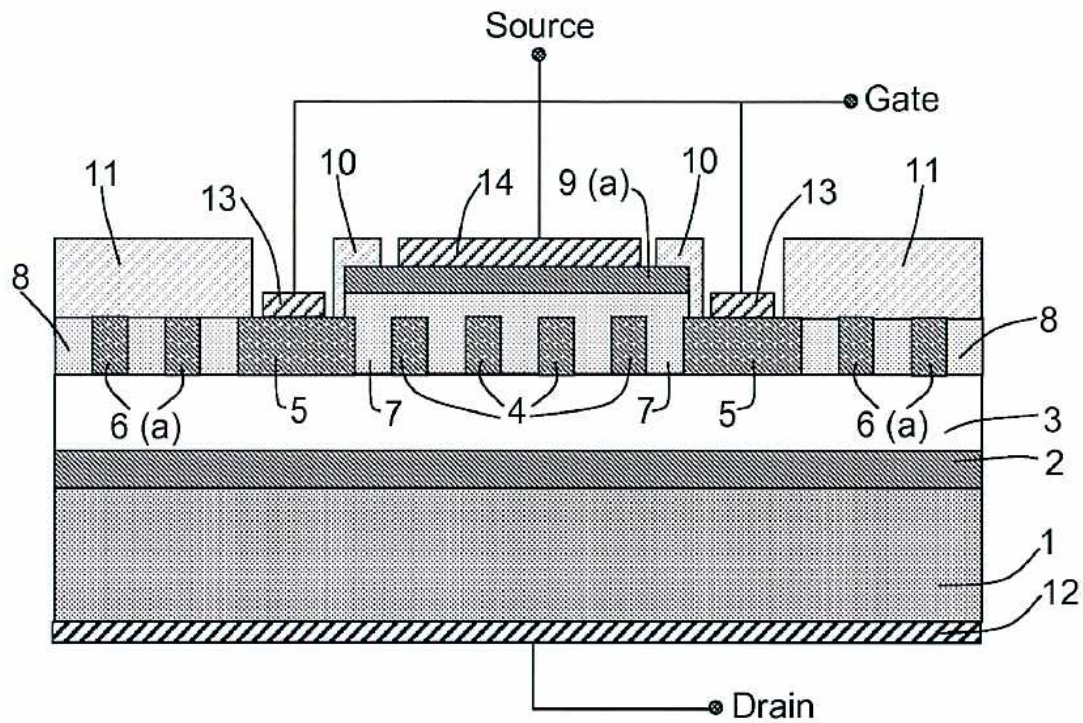
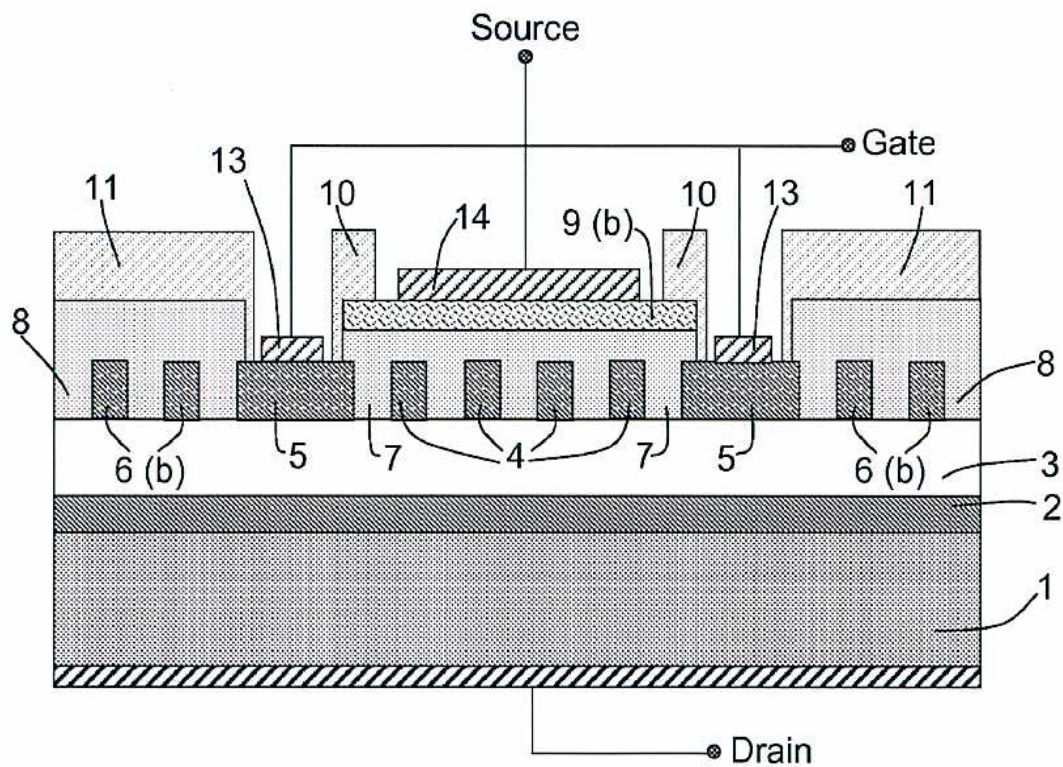
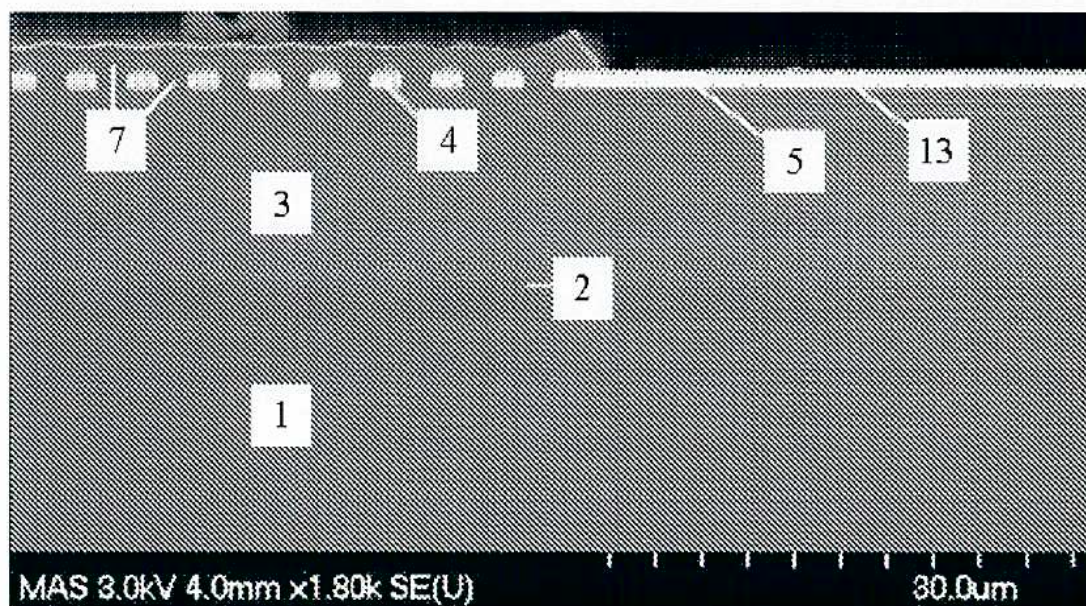
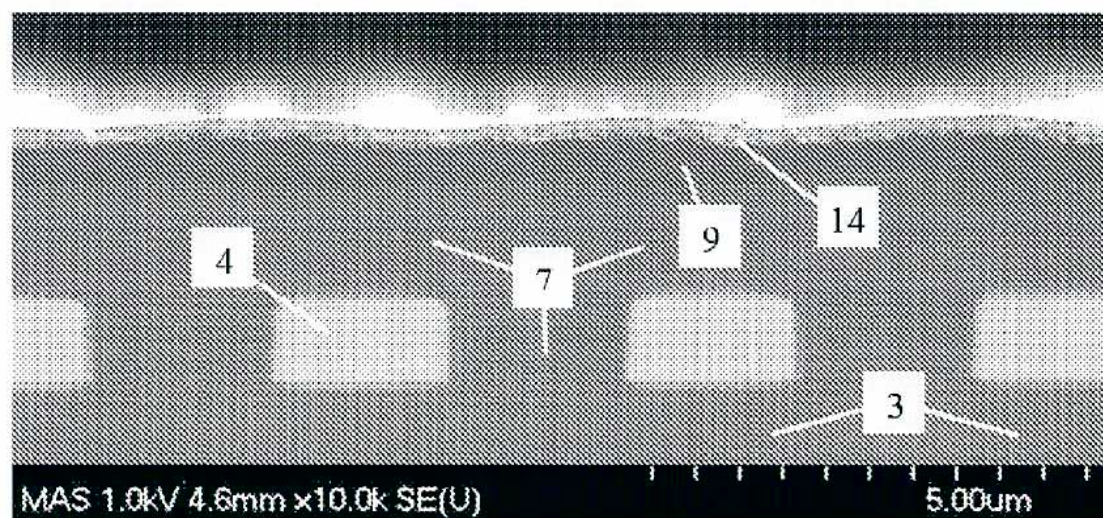
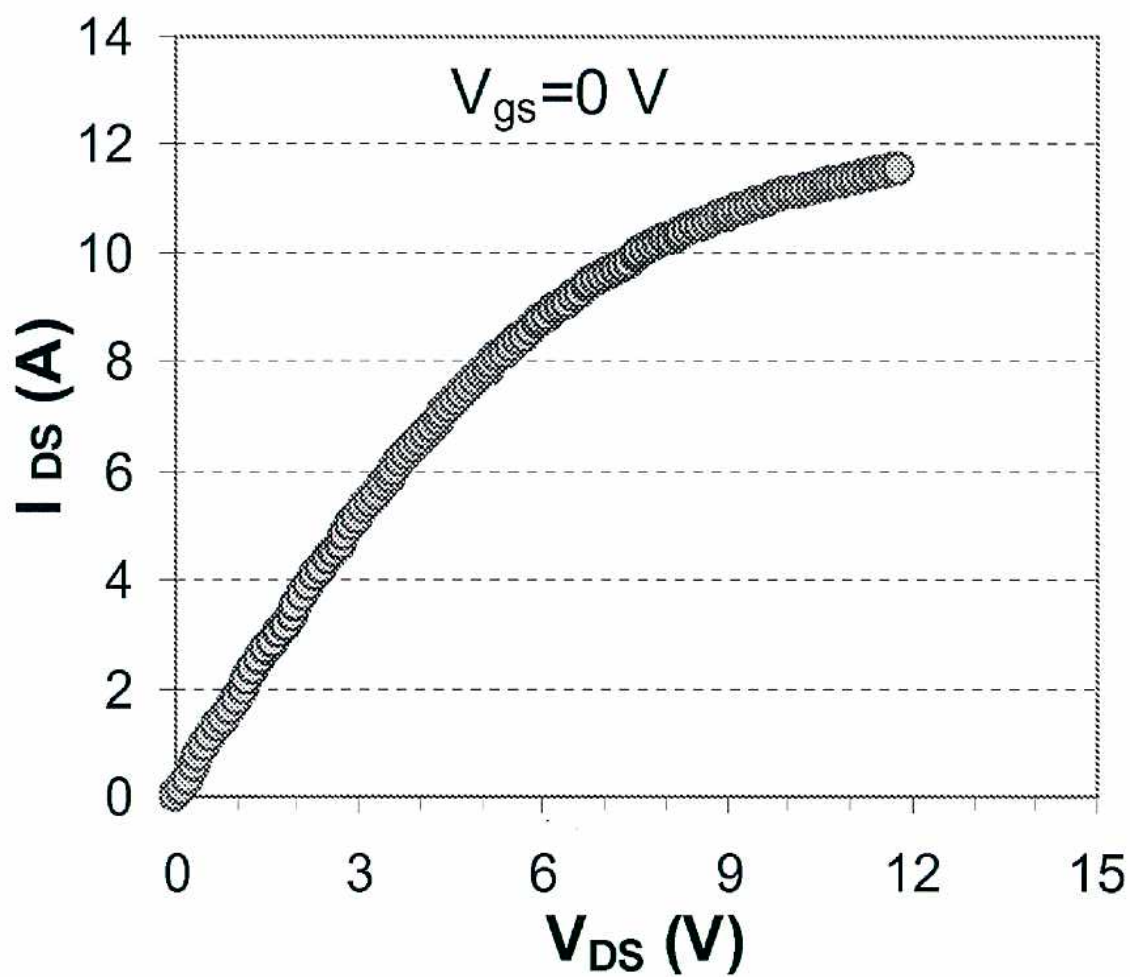
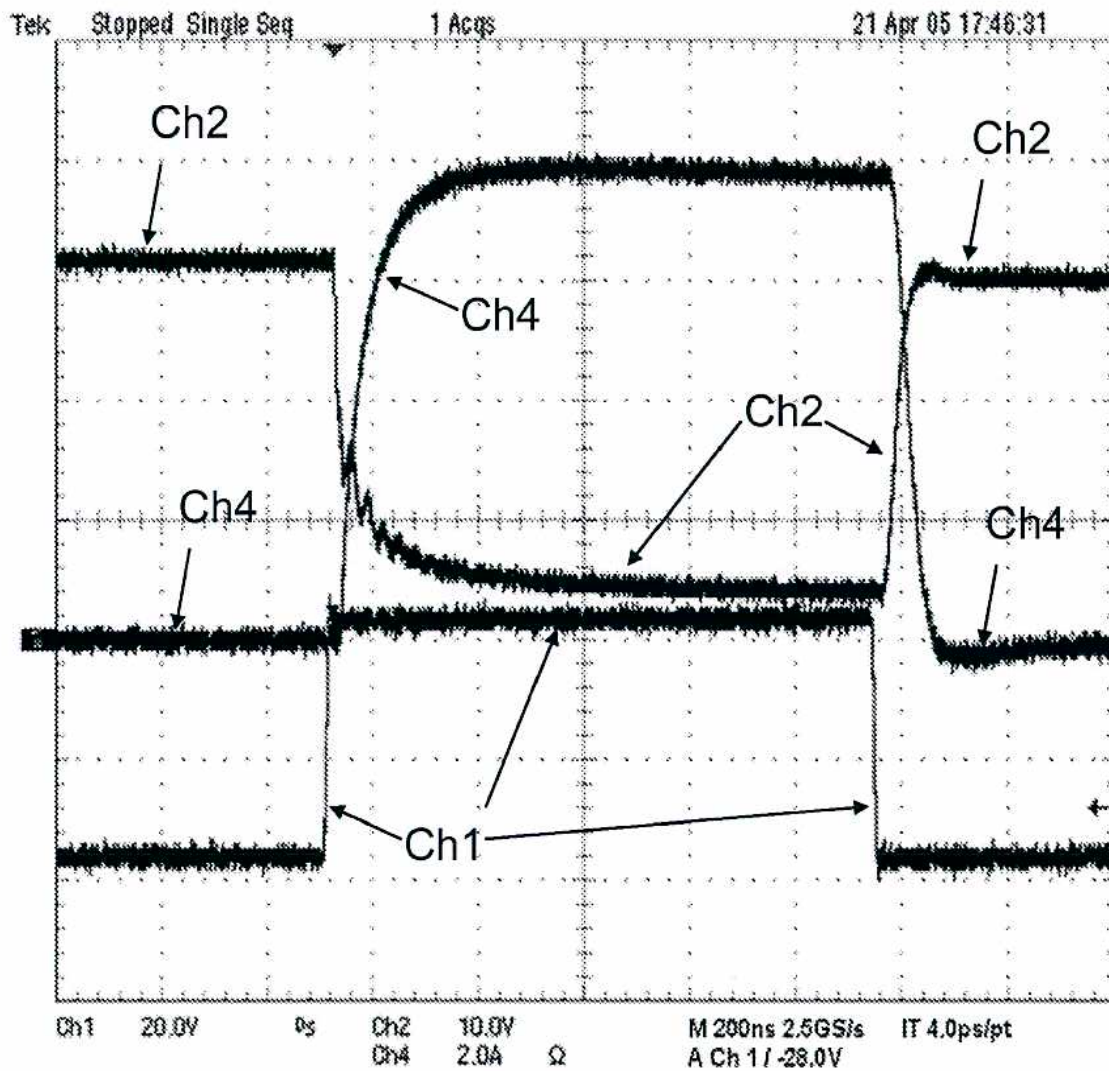


FIG. 8B

**FIG. 9A****FIG. 9B**

**FIG. 10A****FIG. 10B**

**FIG. 11A**

**FIG. 11B**

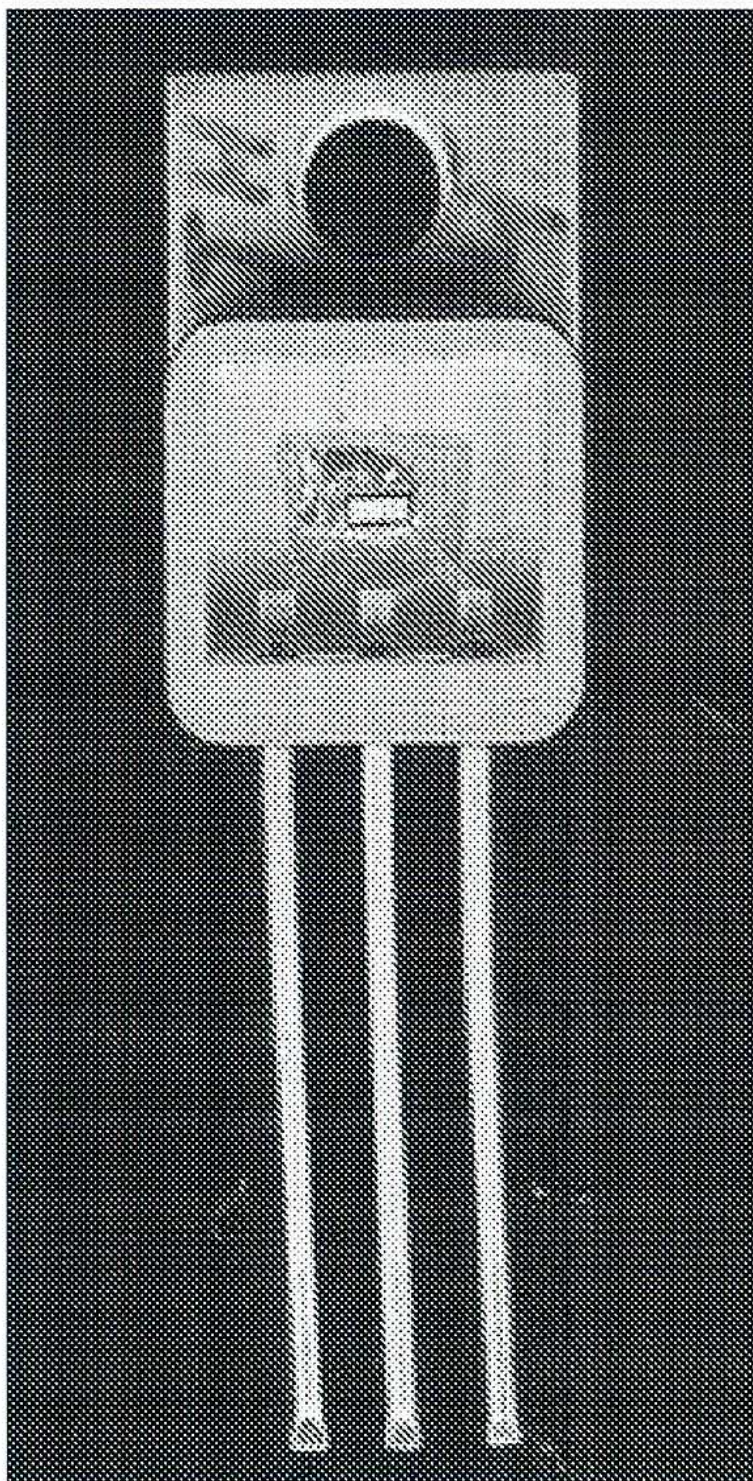


FIG. 12

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VERTICAL-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS HAVING BURIED GATES AND METHODS OF MAKING

CROSS REFERENCE TO RELATED CASES

This application is a divisional of U.S. patent application Ser. No. 11/198,298, filed on Aug. 8, 2005, which is incorporated by reference herein in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

This invention was made with U.S. Government support under F33615-01-D-2103, awarded by the U.S. Air Force Research Laboratory. The U.S. Government may have certain rights in the invention.

BACKGROUND

1. Technical Field

The present application relates, in general, to semiconductor devices and, more particularly, to vertical-channel junction field effect transistors (VJFETs) having buried gates and to methods of making these devices.

2. Background of the Technology

Silicon Carbide (SiC), a wide band-gap semiconductor material, is very attractive for use in high-power, high-temperature, and/or radiation resistant electronics. SiC power switches are logical candidates for these applications due to their excellent material physical properties such as wide energy band-gap, high breakdown field strength, highly saturated electron drift velocity and high thermal conductivity compared to the conventional silicon counterpart. In addition to the above advantages, SiC power devices can operate with lower specific on-resistance than conventional silicon power devices [1].

JFETs in SiC are especially attractive for high power applications thanks to the inherent stability of their p-n junction gate, which is free from gate oxidation problems concerning channel mobility in MOS structure and high-temperature reliability issues in MESFETs having metal-semiconductor Schottky barrier.

Because of the fundamental differences in material properties and processing technologies, traditional Si or GaAs microelectronics technologies in JFETs can not be easily transferred to SiC. A number of reports of SiC JFETs have appeared in the last decade (e.g., [2-4]). An example of a vertical channel JFET employing a recessed gate structure can be found in U.S. Pat. No. 4,587,712 [5]. An example of a lateral JFET formed in SiC can be found in U.S. Pat. No. 5,264,713 [2]. Enhanced-mode JFET for digital ICs with resistive load has been reported in 2000 [6]. JFET-based ICs can also be implemented in either complementary n-type and p-type channels as disclosed in U.S. Pat. No. 6,503,782 [7] or enhanced-depletion (n-type channels) forms. SiC JFETs have proven to be radiation tolerant while demonstrating minimal threshold voltage shift over a wide temperature range [8, 9].

Most of the obstacles to low-cost volume manufacturing can be traced back to the gate-level process steps. In addition, the p-type gate contact can be difficult to fabricate in SiC because of the large band-gap of SiC. In fact, low resistivity contacts to p-type SiC have only been formed on heavily doped p-type SiC.

The VJFET (i.e., a JFET with a vertical channel structure) can be fabricated smaller than a JFET with a lateral channel

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structure, which leads to lower cost in volume manufacturing of discrete transistors, and can also increase the packing density in large scale integrated circuits. To obtain a vertical channel in SiC VJFETs, ion implantation is often used to form the P⁺ gate region [8-10]. It can be difficult, however, to precisely control the channel length by ion implantation because of a combination of uncertainties on actual depth profile of implantation tail, defect density, redistribution of implanted ions after thermal annealing, and ionization percentage of dopant atoms and point defects under different bias and/or temperature stress.

Alternative methods to form a vertical channel have also been employed. One method is to selectively grow P⁺ gate regions epitaxially as taught in U.S. Pat. No. 6,767,783 [11].

There still exists a need, however, for improved high volume, low cost manufacturing methods for VJFETs that allow for the precise control of channel length during manufacture.

SUMMARY

According to a first embodiment, a semiconductor device is provided which comprises:

a substrate layer comprising a semiconductor material of a first conductivity type;

a drift layer on the substrate layer, the drift layer comprising a semiconductor material of the first conductivity type;

a gate region on the drift layer, wherein the gate region comprises a semiconductor material of a second conductivity type different than the first conductivity type;

a channel layer of the first conductivity type on the drift layer and covering a first portion of the gate region; and

a source layer of the first conductivity type on the channel layer.

The drift layer of the device can be on a buffer layer comprising a semiconductor material of the first conductivity type wherein the buffer layer is on the semiconductor substrate. The semiconductor material of the substrate layer, the drift layer, the gate regions and the channel layer can be silicon carbide. The semiconductor material of the first conductivity type can be an n-type semiconductor material and the semiconductor material of the second conductivity type can be a p-type semiconductor material.

According to a second embodiment, a method of making a semiconductor device is provided which comprises:

selectively etching through a gate layer of semiconductor material of a second conductivity type on a drift layer of semiconductor material of a first conductivity type different than the second conductivity type to expose material of the drift layer, wherein the drift layer is on a semiconductor substrate;

depositing a channel layer of semiconductor material of the first conductivity type on exposed portions of the gate and drift layers to cover the gate layer;

depositing a source layer of semiconductor material of the first conductivity type on the channel layer or, alternatively, implanting a source layer of semiconductor material of the first conductivity type in the channel layer;

selectively etching through the channel layer in a peripheral region of the device to expose a portion of the underlying gate layer, wherein an unexposed portion of the gate layer of the device remains covered by the channel and source layers;

depositing a layer of a dielectric material on exposed surfaces of the source layer, the channel layer and the gate layer;

selectively etching through the dielectric layer over the portion of the gate layer exposed during etching of the channel layer to expose underlying gate layer; and

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selectively etching through the dielectric layer over the source layer on the unexposed portion of the gate layer to expose underlying source layer.

The channel layer can be deposited by epitaxial growth on exposed portions of the gate and drift layers. The source layer can be deposited by epitaxial growth on the channel layer or implanted in the channel layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a schematic 2-dimensional illustration of a multi-finger vertical trench JFET with an epitaxially regrown or selectively implanted source region and passivated guard rings.

FIG. 1B is a schematic 2-dimensional illustration of a multi-finger vertical trench JFET with epitaxially regrown or selectively implanted source region and buried guard rings.

FIG. 2 is a schematic diagram of a substrate with epitaxially grown N⁺ buffer, N-type drift, and P⁺ gate layers that can be used in the manufacture of a vertical trench JFET.

FIG. 3 is a schematic diagram of trench-filled P⁺ gate and guard ring regions formed on top of an N-type drift layer.

FIG. 4 is a schematic diagram of the P⁺ gate and guard ring regions of the structure shown in FIG. 3 trench-filled and planarized with N-type channel layer.

FIG. 5A is a schematic diagram of the N⁺ source region homoepitaxially regrown on top of the N-type channel layer of the structure shown in FIG. 4.

FIG. 5B is a schematic diagram of the N⁺ source region selectively implanted in the N-type channel layer of the structure shown in FIG. 4.

FIG. 6A is a schematic diagram of the N-type channel and source regions being patterned and etched back to expose the P⁺ gate pads and guard ring with epitaxially regrown N-type source regions.

FIG. 6B is a schematic diagram of the N-type channel and source regions being patterned and etched back to expose the P⁺ gate pads and guard ring with selectively implanted N-type source regions.

FIG. 6C is a schematic diagram of the N-type channel and source regions being patterned and etched back to expose P⁺ gate pads with buried guard ring and epitaxially regrown N-type source regions.

FIG. 6D is a schematic diagram of the N-type channel and source regions being patterned and etched back to expose P⁺ gate pads with buried guard ring and selectively implanted N-type source regions.

FIG. 7A is a schematic diagram of the dielectric layer(s) being blanket deposited everywhere for both electrical isolation and passivation on top of the epitaxially regrown source and the exposed P⁺ gate pads and guard ring regions.

FIG. 7B is a schematic diagram of the dielectric layer(s) being blanket deposited everywhere for both electrical isolation and passivation on top of the selectively implanted source and the buried guard ring regions.

FIG. 8A is a schematic diagram of the dielectric layer(s) being patterned and etched back to open the metal contact windows on top of the gate and epitaxially regrown source regions.

FIG. 8B is a schematic diagram of the dielectric layer(s) being patterned and etched back to open the metal contact windows on top of the gate and selectively implanted source regions.

FIG. 9A is a schematic diagram of the metals being deposited to form electrically conducting contacts to gate, drain, and epitaxially regrown source regions.

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FIG. 9B is a schematic diagram of the metals being deposited to form electrically conducting contacts to gate, drain, and selectively implanted source regions.

FIG. 10A is a Scanning Electron Micrograph (SEM) of a buried-gate VJFET with self-planarizing epitaxially regrown channel and source regions.

FIG. 10B is a magnified SEM image of a buried-gate VJFET with epitaxially regrown self-planarizing channel and source.

FIG. 11A is a graph showing drain I-V characteristics at zero gate bias for an in-house fabricated VJFET in SiC having homoepitaxially grown drift, buried gate, planarized channel and source regions with 0.5 mm² active area.

FIG. 11B is a switching waveform measured at room temperature for an in-house fabricated VJFET in SiC having homoepitaxially grown drift, buried gate, planarized channel and source regions with 0.5 mm² active area.

FIG. 12 is a photograph of a packaged VJFET in SiC according to one embodiment.

REFERENCE NUMERALS

1. Substrate
2. N⁺ buffer layer
3. N-type drift region
4. P-type buried gate fingers
5. P-type gate pads for metal contacts
- 6(a). P-type passivated guard rings
- 6(b). P-type buried guard rings
7. N-type planarized channel region
8. N-type trench-fill in guard ring regions
- 9(a). Homoepitaxially regrown N-type source region
- 9(b). Selectively implanted N-type source region
10. Isolation dielectric
11. Passivation dielectric
12. Drain metal contact
13. Gate metal contacts
14. Source metal contact

DETAILED DESCRIPTION

An object of the present invention is to provide a vertical-channel Junction Field-Effect Transistor (JFET) with all epitaxially grown drift, buried gate, passivated or buried guard rings, planarized channel with either epitaxially grown or implanted source regions in SiC, that can be made electrically isolated from the other devices fabricated on the same die, and that can be implemented in such a way that the devices fabricated on the same die may have different threshold voltages.

A further object of the invention is to provide the concept and an example of planarization of trench p-gate by homoepitaxial over-growth of channel and source regions on a silicon carbide patterned substrate.

A further object of the invention is to provide the concept and an example of planarization of trench p-gate by homoepitaxial over-growth of only the channel region with the source region formed by implantation on a silicon carbide patterned substrate.

A further object of the invention is to provide a method of the fabrication of the above devices.

The present application relates generally to a Junction Field-Effect Transistor (JFET) with vertical channel. In particular, the present application relates to such transistors formed in silicon carbide (SiC).

The present device is built on a silicon carbide substrate, which can be electrically either p-type or n-type with same type buffer layer. For using the n-type substrate, the device